Difference Amplifier/Common Mode Rejection Ratio

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EGR 214 – Circuit Analysis I

Laboratory Section 04

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Abstract

The purpose of this laboratory is to determine the Common Mode Rejection Ratio (*CMRR*) for a difference amplifier circuit. A difference amplifier is a circuit that will amplify the difference between two input voltages. A circuit schematic was given, and from this schematic the relationship between the input voltages and the output voltages was determined. The circuit was then drawn in P-Spice and simulated. This same circuit was then built using a u741 operational amplifier chip. The *CMRR* was determined algebraically, from the P-Spice model and from the results of measurements using a digital multi-meter. The simulated and experimental results were then compared against the *CMRR* from the mathematical model. While not ideal, the simulated and experimental common mode rejection ratios were extremely close to the mathematically predicted *CMRR*. Because of this the circuit will likely not show any variation in output due to electrical interference.

1.0 Introduction

The difference amplifier is a circuit that requires two separate input voltages. The purpose of the circuit is to amplify the difference between two input voltages. The circuit also has the capability to effectively ignore the inputs when they are the same. This function is vital as all electronic circuits are exposed to interference. Often such interference will result in the input signals having the same voltage value. An ideal difference amplifier will reject all such interference and amplify only the difference between the two inputs.

The key to the difference amplifier is an operational amplifier. Since its inception nearly sixty years ago the operational amplifier has been a key component in computer systems. The internal circuitry in the modern operational amplifier is a complex circuit consisting of resistors, capacitors and inductors. This complex circuit can be considered a black box, which greatly simplifies the analysis of any operational amplifier circuit.

Section 2 outlines the operation of the operational amplifier and the difference amplifier circuit. It also details several properties of the difference amplifier circuit. Section 3 is the analysis of the difference amplifier circuit using assigned nominal resistance values. This section also contains the derivations of the inherent relationships

of the difference amplifier. Section 4 contains a P-Spice simulation of the difference amplifier circuit. Section 5 analyzes the data gathered from the physical circuit. Section 6 is the results discussion section and section 7 is the conclusions section.

2.0 The Operational Amplifier

The Operational Amplifier (OP AMP) is a complex integrated circuit. OP AMPS are amplifying circuits that were originally designed to perform mathematical operations. Early OP AMP consisted of vacuum tubes in early analog computers. As technology evolved, so too did the OP AMP. The most common OP AMP configuration in use today is the 741 integrated circuit chip. Figure 1 shows the 741 chip pin diagram with an OP AMP schematic diagram.

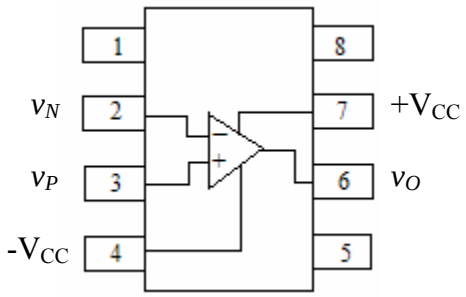

Figure 1: u741 OP AMP Pin Diagram

The OP AMP itself is a five pin device. It is also an active device that depends on present inputs as well as previous inputs to operate. This means that the device requires a voltage to drive it. This voltage is $+V_{CC}$ and $-V_{CC}$, the same voltage with the polarities reversed. These voltages are shown on the pin diagram in Figure 1. Pins 4 and 7 are typically left off of schematic diagrams for the sake of clarity, though the voltages are assumed to be present. The output voltage of the OP AMP cannot exist outside the $\pm V_{CC}$ range. When the output voltage would be less than $-V_{CC}$, the output stays at $-V_{CC}$. This is known as the –Saturation region. Likewise, the output voltage remains at $+V_{CC}$ when it would be greater. This is known as the +Saturation regions. Between the saturation regions the OP AMP is in the linear operation region. The output voltage of the OP AMP in the linear region is determined by

$$v_O = A(v_P - v_N). \tag{1}$$

The relationship of the three regions is shown in Figure 2.

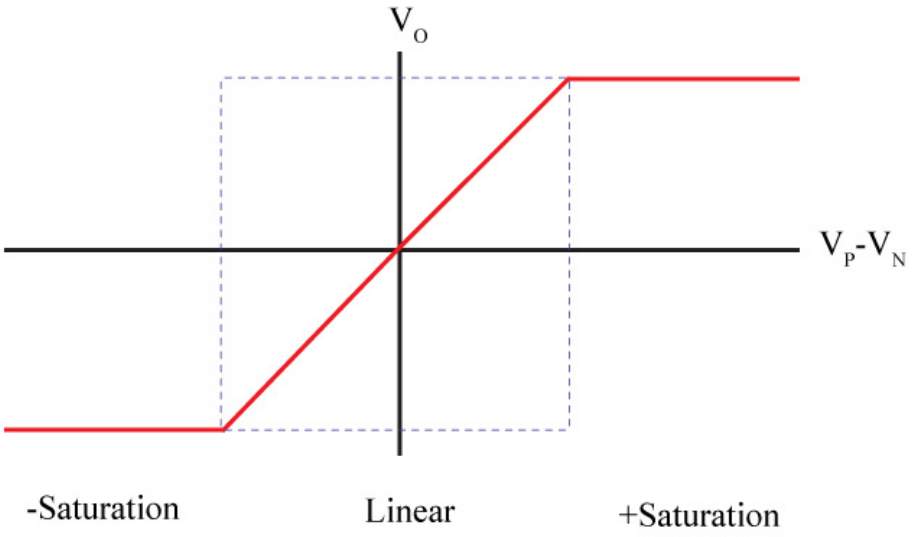

Figure 2: OP AMP Characteristics

The slope of the graph in the linear region is the voltage gain, *A*, from (1). The range of v_O can be used to determine the two main characteristics of an ideal OP AMP. The relationship of v_O to $\pm V_{CC}$ is

$$-V_{CC} \le v_O \le +V_{CC}. \tag{2}$$

When (1) is substituted into (2) the relationship between v_P, v_N and $\pm V_{CC}$ is found to be

$$\frac{-V_{CC}}{A} \le (v_P - v_N) \le \frac{+V_{CC}}{A}. \tag{3}$$

The voltage gain is typically very high in an OP AMP, usually on the order of 10^5. In an ideal OP AMP the gain is assumed to be infinite. When this is the case, the relationship in (3) becomes

$$0 \le (v_P - v_N) \le 0. \tag{4}$$

This shows the first characteristic of an ideal OP AMP. The second characteristic of the ideal OP AMP has to do with currents. The resistance across the two input terminals on an ideal OP AMP is assumed to be infinite. By Ohm's law this means that the current entering both input nodes must be zero. So, the characteristics of an ideal OP AMP are

$$v_P = v_N \tag{5}$$

and

$$i_P = i_N = 0\,. \tag{6}$$

2.1 Difference Amplifier

The difference amplifier is a specific application of the OP AMP. This circuit amplifies the difference between two separate input voltages and ignores common inputs. The schematic for this type of circuit is shown in Figure 3.

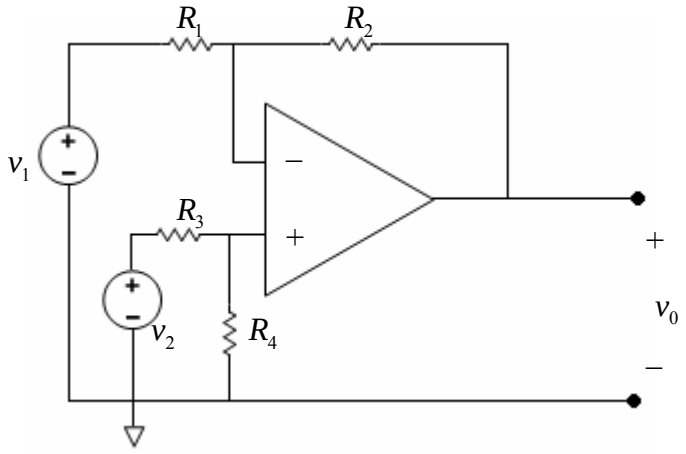

Figure 3: Difference Amplifier Circuit

The relationship of the inputs to the outputs of the difference amplifier can best be described if two new voltages are defined. The differential mode voltage (v_{dm}) and the common mode voltage (v_{cm}) are defined as

$$v_{dm} = v_2 - v_1 \tag{7}$$

and

$$v_{cm} = \frac{v_1 + v_2}{2}\,. \tag{8}$$

These new voltages relate to the output voltages linearly. The new relationship is shown in (9).

$$v_O = A_{cm} v_{cm} + A_{dm} v_{dm} \tag{9}$$

When the two input voltages are the same, they drive the differential mode term to zero. This means that the common mode voltage only shows up in the equation when the two inputs are the same voltage with the same polarity. In order to ensure that this voltage is rejected the common mode gain must be zero. When this happens it can be shown that

$$v_O = 0v_{cm} + \frac{R_2}{R_1} v_{dm} . \tag{10}$$

This relationship shows that any common mode voltage will be disregarded. Likewise any differential mode voltage will be amplified by $\frac{R_2}{R_1}$.

The relationship in (10) holds true only for an ideal difference amplifier. In practical application there are no ideal circuits, however. The common mode gain and the differential mode gain can be used to determine the common mode rejection ratio (*CMRR*). The *CMRR* is a measure of how close the circuit is to being ideal and is stated mathematically as

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right| . \tag{11}$$

A high *CMRR* is the overall goal because a large *CMRR* means that the common mode voltage will have almost no impact on the output voltage. This is necessary because of the nature of the common mode voltage. When the two input voltages have the same value this is typically a result of electrical "noise." A high *CMRR* means that this interference will have very effect on the operation of the circuit.

3.0 Analysis

The overall equation from the schematic in Figure 3 can be used to verify the relationship in (9). This is done using the superposition principle. First, v_2 is suppressed to find the output with respect to v_1. The resulting superposition circuit is shown in Figure 4.

R_1 R_2

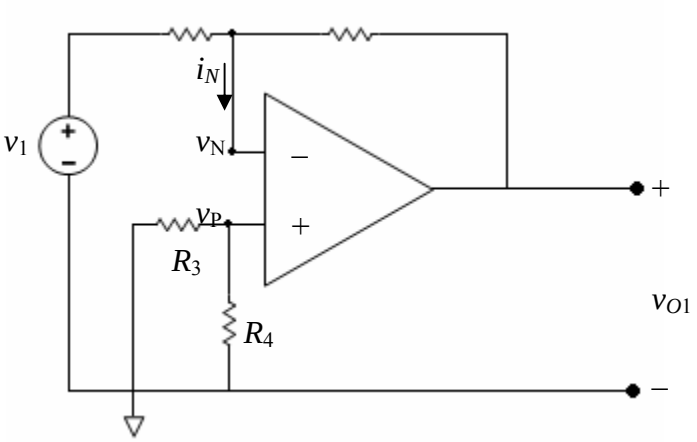

Figure 4: First Superposition Circuit

Figure 1 showed that the voltage entering the negative node of the OP AMP was denoted as v_N and the voltage entering the positive node was v_P. There is no v_P in this superposition circuit so by the relationship in (5) $v_N = v_P = 0$. KCL at the negative OP AMP node can be used to determine the v_O relationship for this circuit.

$$\frac{v_1 - v_N}{R_1} + \frac{v_N - v_{O1}}{R_2} - i_N = 0 \tag{12}$$

When the properties of the ideal OP AMP from (5) and (6) are applied to (12) the relationship for the first output voltage can be found. This derivation is shown in (13), (14) and (15).

$$\frac{v_1}{R_1} + \frac{v_{O1}}{R_2} = 0 \tag{13}$$

$$\frac{v_{O1}}{R_2} = -\frac{v_1}{R_1} \tag{14}$$

$$v_{O1} = -\frac{R_2}{R_1} v_1 \tag{15}$$

Once the relationship for v_{O1} is derived, the second superposition circuit can be solved. This circuit is shown in Figure 5 below.

R_1 R_2

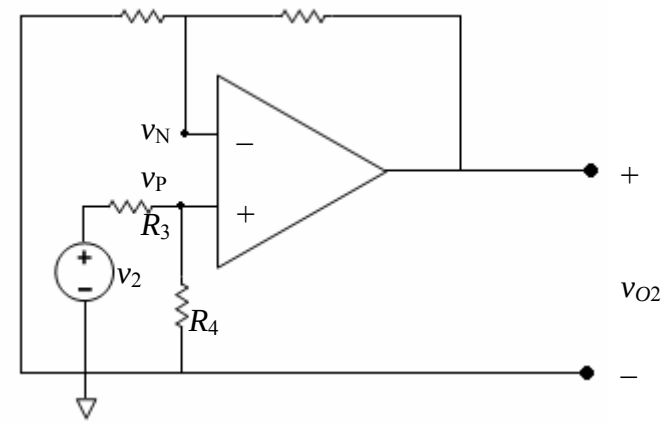

Figure 5: Second Superposition Circuit

By observing Figure 5 it can be seen that v_N and v_P can be found using voltage dividers. These equations are

$$v_N = \frac{R_1}{R_1 + R_2} v_{O2} \tag{16}$$

and

$$v_P = \frac{R_4}{R_3 + R_4} v_2 . \tag{17}$$

Because OP AMPs have the property that $v_P = v_N$, (16) and (17) can be set equal to one another and solved to find the relationship for the second output voltage. This full derivation is shown in (18) through (21).

$$\frac{R_1}{R_1 + R_2} v_{O2} = \frac{R_4}{R_3 + R_4} v_2 \tag{18}$$

$$v_{O2} = \frac{R_4 (R_1 + R_2)}{R_1 (R_3 + R_4)} v_2 \tag{19}$$

$$v_{O2} = \frac{R_2 R_4 \left(1 + R_1 / R_2\right)}{R_1 R_4 \left(1 + R_3 / R_4\right)} v_2 \tag{20}$$

$$v_{O2} = \frac{R_2 \left(1 + R_1 / R_2\right)}{R_1 \left(1 + R_3 / R_4\right)} v_2 \tag{21}$$

The final relationship for v_O is the sum of the superposition solutions, and is stated as

$$v_O = \frac{R_2\left(1+R_1/R_2\right)}{R_1\left(1+R_3/R_4\right)}v_2 - \frac{R_2}{R_1}v_1 . \tag{22}$$

At this point the relationship is in terms of the original input voltages. As shown in section 2.1, the input voltages can be restated in terms of the common and differential mode voltages. From (7) and (8) the values of the input voltages in terms of the mode voltages were determined. These values are

$$v_1 = v_{cm} - \frac{1}{2}v_{dm} \tag{23}$$

and

$$v_2 = v_{cm} + \frac{1}{2}v_{dm} . \tag{24}$$

These values can be substituted into (22) to determine the relationship between v_P, v_N and v_O. The complete derivation of this new relationship is shown below.

$$v_O = \frac{R_2}{R_1}\left(\frac{1+R_1/R_2}{1+R_3/R_4}\right)\left(v_{cm}+\frac{1}{2}v_{dm}\right) - \frac{R_2}{R_1}\left(v_{cm}-\frac{1}{2}v_{dm}\right) \tag{25}$$

$$v_O = \frac{R_2 v_{cm} + R_1 v_{cm}}{R_1 + R_1R_3/R_4} - \frac{R_2 v_{cm}}{R_1} + \frac{R_2 v_{dm} + R_1 v_{dm}}{2\left(R_1 + R_1R_3/R_4\right)} + \frac{R_2 v_{dm}}{2R_1} \tag{26}$$

$$v_O = \left(\frac{R_2+R_1}{R_1+R_1R_3/R_4} - \frac{R_2}{R_1}\right)v_{cm} + \left(\frac{R_2+R_1}{2\left(R_1+R_1R_3/R_4\right)} + \frac{R_2}{2R_1}\right)v_{dm} \tag{27}$$

$$v_O = \left(\frac{R_2+R_1-R_2-R_2R_3/R_4}{\frac{R_1R_4+R_1R_3}{R_4}}\right)v_{cm} + \left(\frac{R_2+R_1+R_2+R_2R_3/R_4}{\frac{2\left(R_1R_4+R_1R_3\right)}{R_4}}\right)v_{dm} \tag{28}$$

$$v_O = \left(\frac{R_1R_4-R_2R_3}{R_1R_4+R_1R_3}\right)v_{cm} + \left(\frac{R_2R_4+R_1R_4+R_2R_4+R_2R_3}{2R_1R_4+2R_1R_3}\right)v_{dm} \tag{29}$$

$$v_O = \left(\frac{R_1 R_4 - R_2 R_3}{R_1 (R_3 + R_4)} \right) v_{cm} + \left(\frac{R_4 (R_1 + R_2) + R_2 (R_3 + R_4)}{2R_1 (R_3 + R_4)} \right) v_{dm} \tag{30}$$

This final relationship fits the form shown in (9). The coefficient term on the common mode voltage is A_{cm} and the coefficient on the differential mode voltage is A_{dm}. The ideal difference amplifier will reject all common mode voltages. This only occurs when R_1=R_3 and R_2=R_4. When this relationship is substituted into (30) the resulting relationship matches (10).

Specific resistor values were assigned for use in this experiment. The nominal resistor values used are shown in (31).

$$\begin{aligned} R_1 &= 1k\Omega \\ R_2 &= 23k\Omega \\ R_3 &= 1k\Omega \\ R_4 &= 22k\Omega \end{aligned} \tag{31}$$

Using these values for the resistors, $R_2 \neq R_4$. This means that the difference amplifier in this laboratory will not be ideal and there will be some common mode gain. A small common mode gain is acceptable in the performance of the difference amplifier as long as the difference mode gain is large. This will result in a large *CMRR* and will still allow the circuit to operate with little interference from electrical "noise."

The resistor values in (31) can be substituted into (30) to determine the common mode and differential mode gains. These resulting gains are

$$A_{cm} = -0.045043 \tag{33}$$

and

$$A_{dm} = 22.8789\,. \tag{34}$$

The relationship of v_O, v_{cm} and v_{dm} then becomes

$$v_O = -0.045043 v_{cm} + 22.8789 v_{dm}\,. \tag{35}$$

The three-dimensional plot of this is shown in Figure 7.

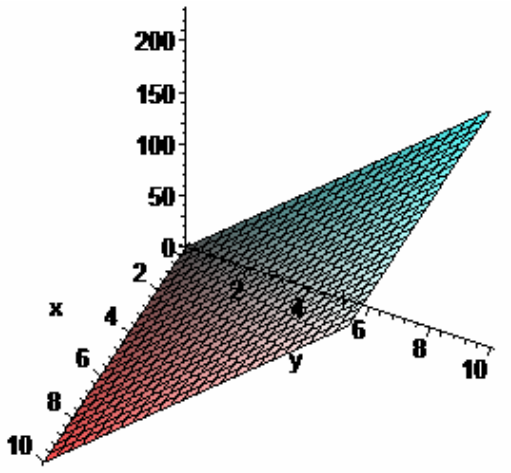

Figure 7: 3-D Plot of v_O using analysis data

Figure 7 shows that while (35) is not ideal, there is very little change due to v_{cm} meaning the impact it has on the equation is negligible. The *CMRR* for this model is

$$CMRR = \left| \frac{22.8789}{-0.045043} \right| = 507.93464 . \tag{36}$$

Because this *CMRR* only involves nominal resistor values (36) will be the standard against which the simulated and experimental results will be checked.

4.0 Simulation

The resistor values in (31) were input into P-Spice. There were two separate sets of simulations run: one set where $v_1 = v_2$ and one set where $v_1 = -v_2$. For the first set the v_{dm} term in (9) became zero. For the second set the v_{cm} term in (9) became zero. An example of the P-Spice results for one of the simulations is shown in Figure 8.

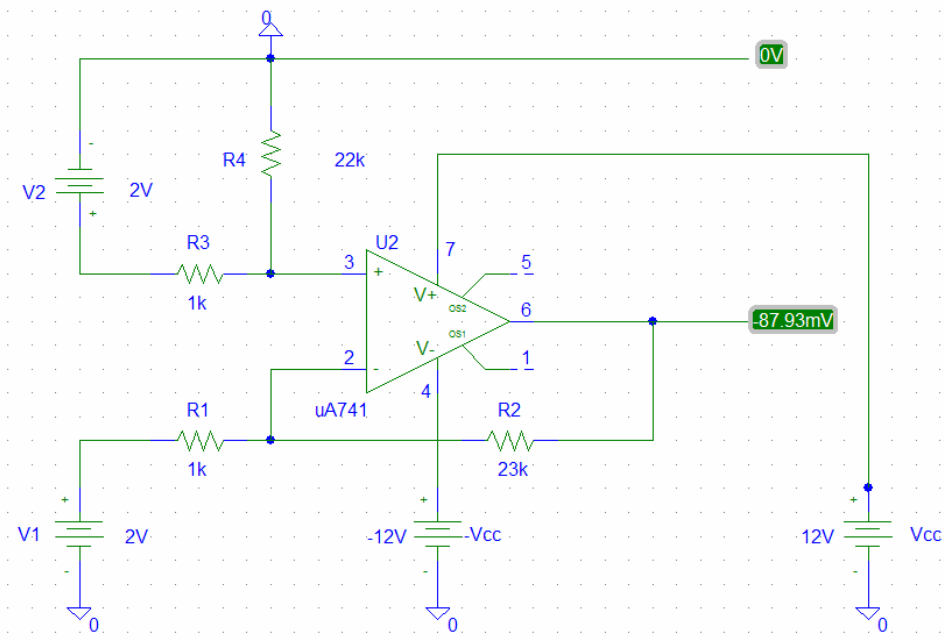

Figure 8: P-Spice Simulation Schematic ($v_1 = v_2 = 2V$)

The results of the P-Spice simulations for $v_1 = v_2$ are given in Table 1. The common and differential mode voltages were found by substituting the values of v_1 and v_2 into (7) and (8). The common mode gain was calculated by substituting the values for v_{cm}, v_{dm} and v_O into (9).

Table 1: Common Mode Gain Simulation Results

v_1 (V)	v_2 (V)	v_{cm}	v_{dm}	v_O (mV)	A_{cm}
1	1	1	0	-47.73	-0.04773
2	2	2	0	-87.93	-0.043965
3	3	3	0	-132.12	-0.04404
4	4	4	0	-176.31	-0.044078
5	5	5	0	-220.49	-0.044098
6	6	6	0	-264.67	-0.044112

The data in Table 1 was input into a Microsoft Excel spreadsheet. The common mode voltage was then plotted against v_O and a linear regression was performed. This plot is given in Figure 9.

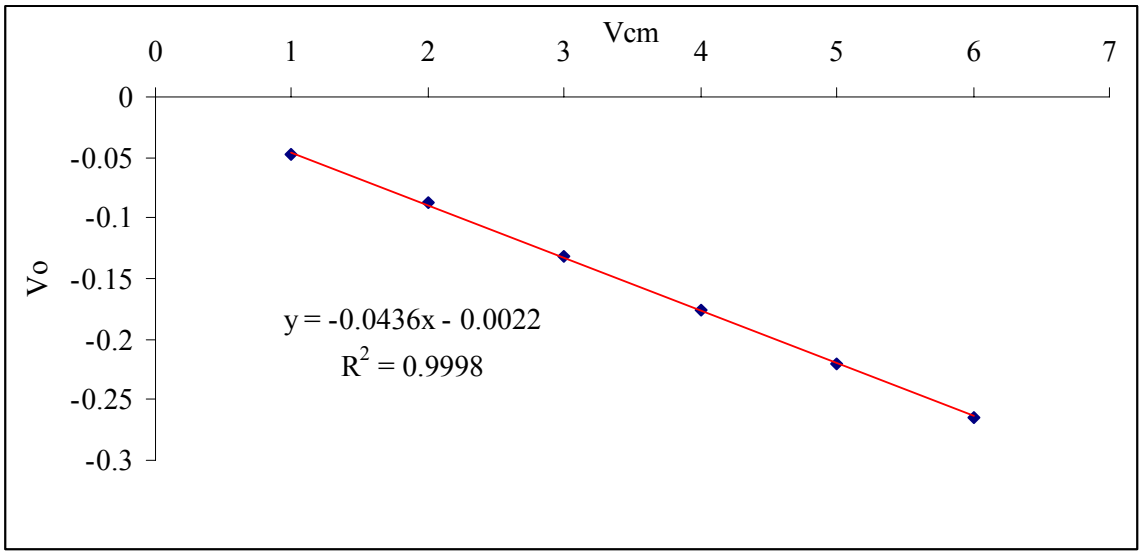

Figure 9: v_{cm} vs. v_O for the simulated common mode gain

The common mode gain is the slope of the v_{cm} vs. v_O trend line. Figure 8 shows that the common mode gain for the simulated results was -0.0436. This was the common mode gain used in determining the relationship of v_O to the common mode and differential mode voltages.

After the simulations to determine the common mode gain, the simulations for the differential mode gain were run. Again the values for v_{cm}, v_{dm} and v_O were substituted into (9) to determine the gain. The simulation results are shown in Table 2.

Table 2: Differential Mode Gain Simulation Results

v_1 (V)	v_2 (V)	v_{cm}	v_{dm}	v_O (V)	A_{dm}
-0.01	0.01	0	0.02	0.45997	22.9985
-0.02	0.02	0	0.04	0.91947	22.9868
-0.03	0.03	0	0.06	1.379	22.9833
-0.04	0.04	0	0.08	1.839	22.9875
-0.05	0.05	0	0.10	2.298	22.98
-0.06	0.06	0	0.12	2.758	22.9833

This data was again input into an Excel spreadsheet. The resulting plot with trend line is given in Figure 10.

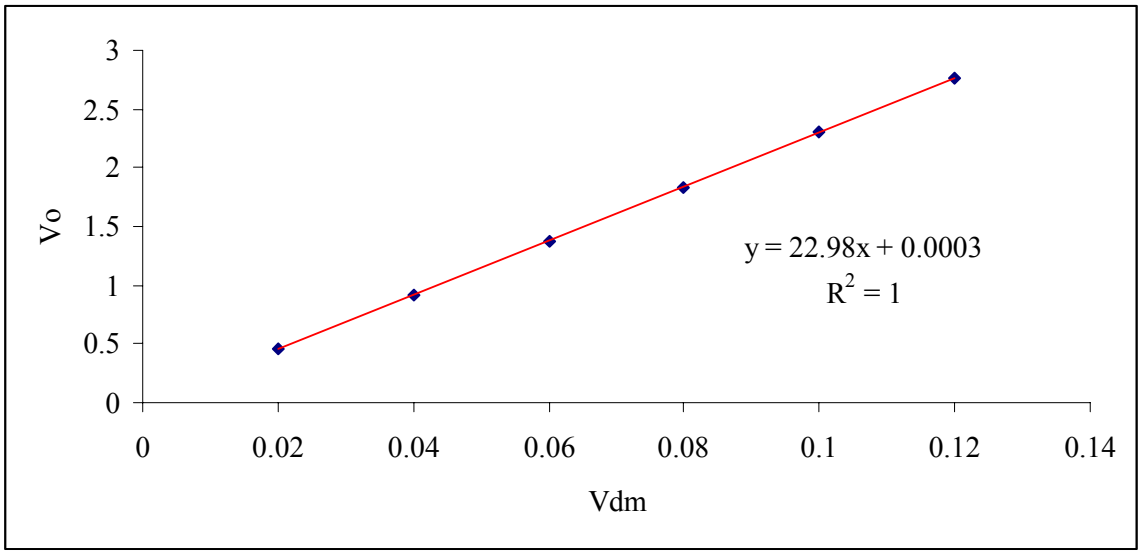

Figure 10: v_{dm} vs. v_O for the simulated differential mode gain

Again, the slope of the plot shown in figure t is the differential mode gain. Both of the gains determined in the regressions were input into (9) in order to determine the relationship for the simulation data. This relationship was found to be

$$v_O = -0.0436v_{cm} + 22.98v_{dm}. \tag{37}$$

This equation was then graphed on a three dimensional coordinate system. The resulting graph is shown in Figure 11.

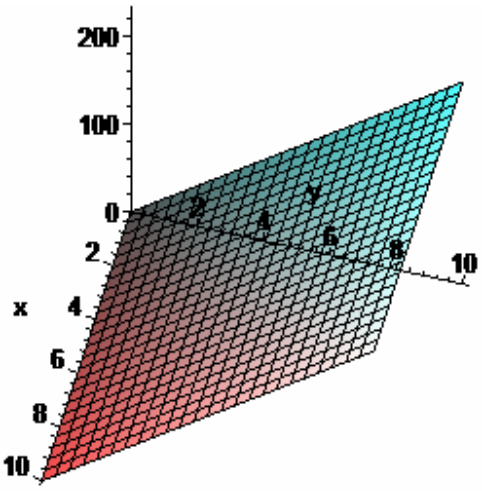

Figure 11: 3-D Plot of v_O using simulated data

The *CMRR* for the simulation data was

$$CMRR = \left| \frac{22.98}{-0.0436} \right| = 527.064 \,. \tag{38}$$

5.0 Experimental Results

Four resistors with nominal values shown in (31) were chosen. The actual resistances were measured and recorded in Table 3.

Table 3: Resistor Values

Resistor	Nominal Value ($k\Omega$)	Measured Value ($k\Omega$)
R_1	1	0.994
R_2	23	22.764
R_3	1	0.994
R_4	22	21.74

The circuit in Figure 3 was built on the CADET circuit trainer using the resistors in Table 3. The first set of data measured was used to determine A_{cm}. To do this the input voltages were equal to one another. This makes the differential mode voltage zero. The values were then substituted into (9) and solved for A_{cm}. The results of these measurements and calculations are given in Table 4.

Table 4: Common Mode Gain Experimental Results

v_1 (V)	v_2 (V)	v_{cm}	v_{dm}	v_O (mV)	A_{cm}
1.01	1.01	1.01	0	-0.038	-0.037624
2.00	2.00	2.00	0	-0.077	-0.0385
3.057	3.057	3.057	0	-0.101	-0.033039
4.08	4.08	4.08	0	-0.138	-0.033824
5.03	5.03	5.03	0	-0.179	-0.035586
6.08	6.08	6.08	0	-0.215	-0.035362

The experimental data was then input into an Excel spreadsheet. A regression analysis was performed. The resulting plot is shown in Figure 12.

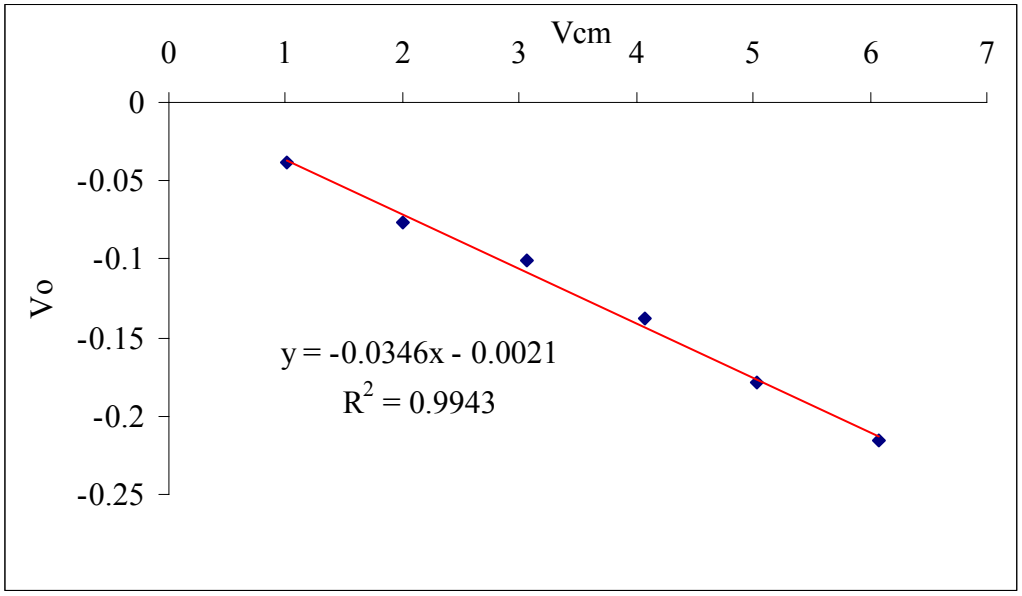

Figure 12: v_{cm} vs. v_O for the experimental common mode gain

Again, the common mode gain will be the slope of the trend line in Figure 12. The common mode gain for this experiment was -0.0346. The same type of process was used for the differential mode data in Table 5.

Table 5: Differential Mode Gain Experimental Results

v_1 (V)	v_2 (V)	v_{cm}	v_{dm}	v_O (V)	A_{dm}
4.98	5	4.99	0.02	0.942	55.733
4.80	5	4.9	0.2	4.97	25.698
4.68	5	4.84	0.32	7.47	23.867
4.47	5	4.735	0.53	11.32	21.668
4.28	5	4.64	0.72	11.32	15.945
4.84	5	4.92	0.16	3.91	25.501

In this experiment, it was impractical to use equal but opposite voltages for v_1 and v_2. There were two difficulties with the original set-up. First, if a single power supply was used to provide the opposite voltages the supply would be shorted. This had the potential of damaging the power supply. The second difficulty came if two supplies were used to provide the opposite voltages. This meant that the power supplies would have had to have been moved from one lab station to another. This method would have been impractical. It was determined that since there was no practical way to provide the necessary equal and opposite voltages, the voltages would be chosen sufficiently close to one another so that the common mode voltage would be nearly constant. The gain could be calculated using the common mode gain, the common mode voltage and the differential mode voltage as in the previous data set. The data in Table 5 was again input into Excel and a linear regression was performed. This regression plot is shown in Figure 13.

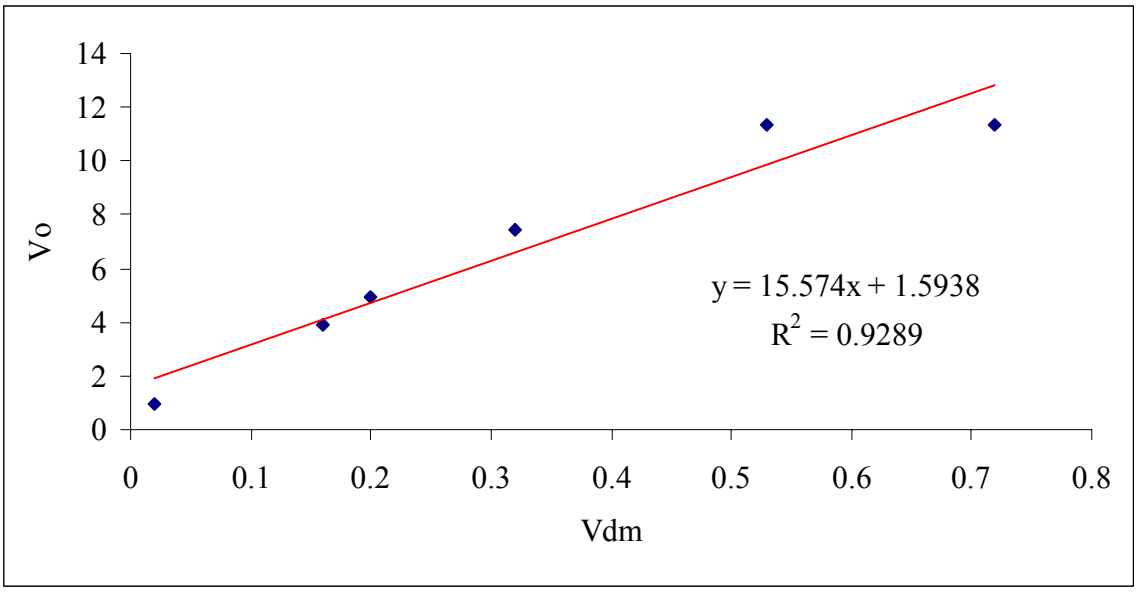

Figure 13: v_{cm} vs. v_O for the experimental differential mode gain

The R^2 value of the regression line in Figure 13 seemed too low for an accurate best-fit line. The data was checked, and it was determined that the circuit was saturating when the difference mode voltage was approximately 0.5. This was found to be the two data points that resulted in v_O=11.32. These two data points were left out of the regression model, resulting in Figure 14.

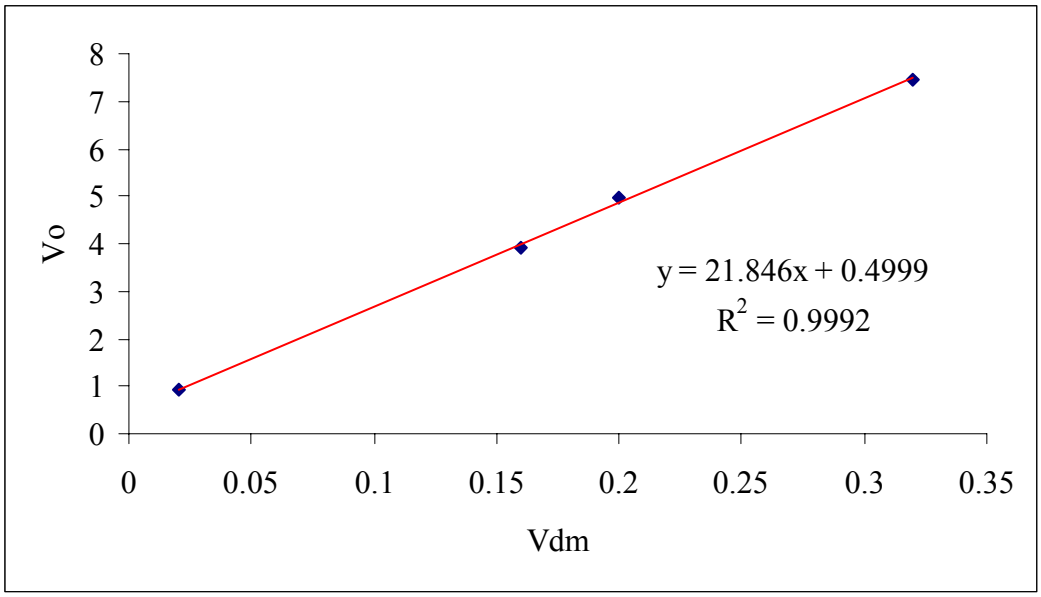

Figure 14: Modified v_{dm} regression plot

The R^2 value in Figure 14 was much higher than that in Figure 13 meaning that the regression line is a better fit. The model in Figure 14 was the A_{dm} value used for the v_O equation. The experimental v_O equation was

$$v_O = -0.0346 v_{cm} + 21.846 v_{dm} . \tag{39}$$

This equation was then used in generating the three dimensional graph of v_O. This graph is given in Figure 15.

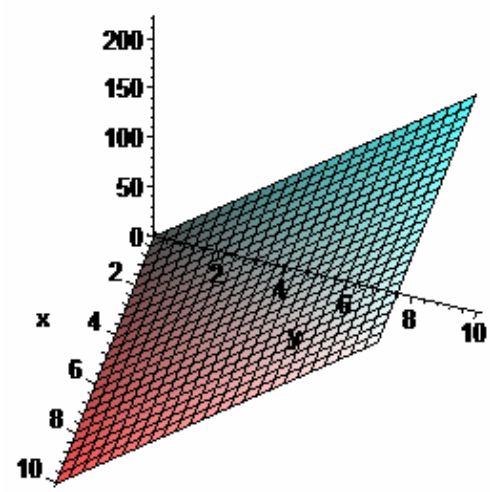

Figure 15: 3-D Plot of v_O using experimental data

Finally, the *CMRR* for the experimental data was calculated in (40).

$$CMRR = \left| \frac{21.846}{-0.0346} \right| = 631.387 \tag{40}$$

6.0 Discussion

The *CMRR* based solely on the nominal resistance values in the circuit was approximately 507. The *CMRR* calculated in section 4 was approximately 527, and the *CMRR* from the experimental data was approximately 631. These values were all large enough to conclude that outside electrical interference will not have any effect on the operation of the circuit.

This is supported by the 3-D graphs in each section. Each of these plots showed very little change due to the x-variable, v_{cm}. This suggests that in each of the equations, the common mode gain was nearly zero. In fact, when arbitrary values were chosen for v_{cm} and v_{dm} it required an increase of nearly 1000 volts in v_{cm} to create a noticeable difference in v_O.

The only discrepancy in the results of each model is in the *CMRR* for the experimental data. This value was greater than the other two by approximately 100. There were two possible explanations for this difference. The main reason was the resistor values. The analysis and simulation *CMRR*s assumed that the resistances were all equal to the nominal value. For the experimental *CMRR*, the resistances varied within the allowable ±5% tolerance rating. This variance was likely large enough to cause a good portion of the difference. The second reason for the difference between *CMRR*s was the method in which the experimental v_{dm} data was collected. In the ideal model, the common mode gain is zero. In turn, since the common mode gain in the experimental calculations was known to be non-zero the common mode voltage would have had to have been zero. This proved impractical in the lab. Instead it was proposed that if v_1 and v_2 were kept close enough together the common mode voltage could be assumed to be constant. This assumption is the second source of error. The common mode voltage was nearly constant but there was some amount of variation.

7.0 Conclusions

The difference amplifier circuit is a circuit that amplifies the difference between two input signals. A mathematical model for the relationship of the output voltage to the input voltage was derived in section 3.0. This model was used as the standard against which the simulated and experimental results were checked. Because of the overall precision in the three different common mode rejection ratios the results of the experiment verify the characteristics of the ideal difference amplifier, also discussed in section 3.0. In addition, the *CMRR* for all three sections was high enough to be reasonably certain that electrical "noise" will not have any noticeable effect on the output of the difference amplifier circuit.